REMARKS

Claims 1-32 are pending and all have been rejected under 35 U.S.C. §§ 102 and 103, and also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of co-pending Application number 10/044364. Applicants are amending claims 1, 5, 6, 9-14, 17, 18, 20-24, 27, 28, and 30-32, canceling claims 3, 4, 15, 16, 25, and 26, and adding claims 33-35.

In paragraph 1 of the Office Action, Applicants were reminded of the duty to fully disclose information under 37 CFR 1.56. Such reminder is very much appreciated.

In paragraph 3, it was indicated that the Specification had not been checked for all possible minor errors. To the best of Applicants' knowledge, the Specification does not include any typographical errors, and showing such errors with specificity would be very much appreciated.

In paragraph 4, claim 1 was objected to because of informalities. The recitation of "determining the access time" should be changed to "determining an access time." Claim 1 is being amended including the change. Withdrawal of the objection is respectfully requested.

In paragraph 5, claims 1-32 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unptentable over claims 1-25 of co-pending Application No. 10/044364. It was indicated that "[a]lthough the conflicting claims are not identical, they are not patentably distinct from each other because both memory system comprise substantially the same elements of a system and method for managing a memory system . . . ." The set of claims in this application is being amended to include limitations distinguished from

claims 1-25 in the co-pending application, and therefore withdrawal of this rejection is solicited.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102 – Hughes

In paragraphs 6 and 7, claims 1-2, 13-14, and 23-24 were rejected under 35 U.S.C. § 102 (b) as being anticipated by U.S. patent number 5,784,582 to Hughes ("Hughes"). It is respectfully submitted that Hughes does not anticipate the claimed invention because it does not disclose every limitation of the claimed invention, and the rejection is therefore traversed.

The Office Action asserted "Hughes discloses a system and method for managing access latency by prioritizing memory access requests among a plurality of data paths based on configuration parameters, wherein the configuration parameters comprise location, size and direction of the transfer in combination with information of the current request." While this assertion is true, it does not show that the claimed invention is being anticipated by Hughes

Regarding claims 1 (and 23), the Office Action asserted:

> Hughes discloses a system and method substantially as claimed comprising the steps of: upon accessing the memory system for a piece of data used by a first process [i.e., request] determining an access time to acquire the piece of data in the memory system; comparing [i.e., selecting] the determined access time to a threshold [i.e., based on the parameter provided to the selection processor by the control state registers 109 (Figure. 3; column 5, lines 46-48)]; and taking actions based on the results of the comparing step; wherein accessing the subsystems is in a non-sequential order [i.e., selecting request according to the parameters including location, size and direction of the transfer of the current access (Figure 4; column 2, lines 10-43]; column5 [sic], line 63 through column 6, line 5; and column 6, lines 46-49]

The Office Action failed to show that claim 1 (and 23) is anticipated by Hughes. The Office Action failed to show complete correspondence between the claim limitations and the teaching of Hughes, and therefore failed to establish that the claim is anticipated. In general, claim 1 includes limitations comparing an access

time to acquire a piece of data to a threshold and taking an action based on results of such comparison. In contrast, Hughes is about prioritizing the requests for access to the shared memory system.

The Office Action failed to show the limitation of "upon accessing the memory system for a piece of data used by a first process, determining an access time to acquire the piece of data in the memory system." While Hughes discloses "requests" for access to the shared memory, it does not teach, suggest, or make obvious "determining *an access time to acquire the piece of data* in the memory system" (emphasis added).

The correspondence of the claimed "comparing the determined access time to a threshold" to "i.e., selecting" and "i.e., based on the parameters provided to the selection processor 108 by the control state registers 109" is mistaken. The Office Action failed to indicate what was being selected. The Office Action failed to show a threshold. The Office Action failed to show the "determined access time." Consequently, the Office Action also failed to show "comparing the determined access time to a threshold." Further, as currently amended, the limitation that "a value of the threshold is selected based on whether the value is a realistic time for a memory access" is not disclosed in Hughes.

Hughes' cited Fig. 3 shows a block diagram of a shared memory arbiter/controller (col. 3, lines 42-43). Hughes' col. 5, lines 46-48 recite "[t]he request selection processor 108 is coupled to the control state registers 109 to provide parameters for the selection process." Both recitations including the parameters for the selection process of the request to access memory have no bearing on the claimed access time, the threshold to be compared with the access time, etc.

The correspondence of Hughes' "selecting a request for access to the shared memory based on the parameter provided to the selection processor 108 by the control

registers 109" to the claimed "comparing the determined access time to a threshold," failed because, as can bee seen, "selecting a request for access to the shared memory" and the claimed "comparing the determined access time to a threshold" have no patentably relationship to one another. Hughes' parameters have no bearing on the claimed access time (for the piece of data) or the threshold to be compared with that access time. Hughes' parameters are used for selecting and prioritizing requests and include location, size, and direction of the transfer in combination with information of the current request to reduce access latency. Hughes' parameters help reduce access latency but do not correspond to the claimed access time. Further, the claimed invention is not about reducing access latency as in Hughes, but includes taking actions based on results of comparing the access time to a threshold.

Hughes' Fig. 4 is a flowchart illustrating the process executed in the shared memory arbiter (col. 3, lines 45-46) in which the controller receives multiple requests for access to the shared memory. If more than one request has the highest priority, then a process is executed to select the optimum request. However, if only one request has the highest priority, then the highest priority request is selected (col. 6, lines 63-66). Hughes' cited col. 2, lines 10-43 is part of the summary discussing "a shared memory architecture" (col. 2, lines 11-12) in which the shared memory generates requests for access to the shared memory. The requests have characteristics including a starting address, a length and an access type, which are processed in a memory controller. In one aspect, the memory controller includes logic responsive to configuration parameters to control the data paths sharing the memory. The configuration parameters comprise a data path priority parameter to manage the latency of stored requests from the plurality of data paths. A data path can be given highest priority and be processed ahead of requests from other data paths, and thus provides protection to the high priority data path to ensure best case access to the

shared memory. These cited paragraphs have no bearing on the claimed invention including limitations such as an access time to acquire the piece of data in the memory system, comparing the determined access time to a threshold, a value of the threshold is selected based on whether the value is a realistic time for a memory access, etc.

Controlling the priority of data paths sharing the memory in Hughes has nothing to do with determining the access time to acquire the piece of data in the memory system, or comparing the determined access time to a threshold, or taking actions based on results of the comparing step.

Neither does Hughes disclose the following limitations

"a value of the threshold is selected based on whether the value is a realistic time for a memory access;

a memory table includes entries pointing to data blocks storing data for at least one subsystem;

the entries are used to locate the data stored in the data blocks; and

while the first process is being executed, the memory table working with a memory manager manages the data blocks independent of an operating system working with the memory system and independent of a processor working with the memory system"

Because the limitations of claims 3 and 4, which were rejected based on the combination of Hughes with U.S patent number 5,297,265 to Frank ("Frank"), are now in claim 1 and 23, Frank is now addressed. Frank does not provide the limitations not taught in Hughes, and the alleged motivation for combining the teachings of Hughes and Frank is improper. Therefore, the claimed invention is distinguished from Hughes and Frank, either alone or in combination.

For example, Frank does not disclose a threshold to be compared with the access time. Frank does not disclose the value of the threshold is selected based on whether the value is a realistic time for a memory access.

Frank does not disclose a memory manager. Frank does not disclose "the memory table working with the memory manager manages the data blocks." Frank does not disclose such management of the data blocks is "independent of an operating system working with the memory system and independent of a processor working with the memory system" while the first process is being executed.

The assertion that "it would have been obvious . . . to implement the system and method for managing a memory system as taught by Hughes to utilize a memory table as taught by Frank to improve data coherency, which requires little or no software overhead, as well as reducing memory access latency and bus contention providing a multiprocessing system with unlimited scalability as pointed out by Frank on column 2, line 27 through line 37" is improper because it is merely a broad conclusory statement and no evidence that suggests the combination was provided. The assertion is a recitation of Frank that does not suggest the motivation for combining the teaching of Hughes and Frank. Therefore, the alleged motivation is insufficient to support a prima facie case of obviousness.

Regarding claims 2 and 24, the Office Action cited Hughes' Figure 4, column 5, lines 63 through column 6, line; and column 6, lines 46-49. These cited paragraphs do not disclose the data block containing the piece of data is placed in the memory system based on information selected in one or a combination of a movement pattern of data in the data block, a structure of the memory system, and a cache-level architecture in the memory system. In fact, the Office Action admitted that these paragraphs of Hughes are about "selecting request according to the parameters including location, size and direction of the transfer of the current access." Those

skilled in the art will recognize that placing the data blocks in the memory is patentably distinguished from selecting the request to access the shared memory.

Regarding claims 13-14, the Office Action asserted that "Hughes teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102 – Lamberts

In paragraph 8, claims 1-2, 13-14 and 23-24 were rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. patent number 6, 418,510 to Lamberts ("Lamberts"). Lambert does not anticipate the claimed invention because Lamberts does not disclose every element of the claimed invention.

The Office Action alleged that "Lamberts discloses a system and method for memory management that makes cache decisions based on a cost function wherein the cost function is calculated as a function of cache access time. Data with higher cost (i.e., higher access time) is added or kept in the cache while data with lower cost (i.e., lower access time) is not stored in the cache." While this assertion is true, the claimed invention is not anticipated by this teaching.

Lamberts does not anticipate the claimed invention that includes limitations such as determining an access time, comparing the determined access time to a threshold, wherein a value of the threshold is selected based on whether the value is a realistic time for a memory access, etc. Lamberts discusses the cost functions including the disk access time, and the cost functions are compared against one another. In contrast, the claimed access time is compared to a threshold wherein a

value of the threshold is selected based on whether the value is a realistic time for a memory access.

Regarding claim 1 and 23, the Office Action cited FIG. 3, references 58 and 60; FIG. 4, references 90 and 92; FIG. 3 elements 62 and 66; FIG. 4, references 94 and 98; FIG. 3, references 64, 68, 70, and 72; FIG. 4 references 96, 100, 102, and 104; and col. 4 lines 29-55.

The cited FIG. 3, references 58 and 60 are about calculating a cost function for writing data block to disk; calculating the cost function for each data block currently stored in the cache. The cited FIG. 4, references 90 and 92 are about calculating the cost function for not storing the data in cache and calculating the cost function for replacing each cached data block. The cited FIG. 3, elements 62 and 66 are about comparing the cost function for the new data block to the cost function for the cached data block. The cited FIG. 4, reference 94 and 96 are about comparing the cost function for the new data block to the cost function for the cached data block and not storing the new data block in cache if the cost function of the new data block has a lower cost function.

The cited FIG. 3, references 64, 68, 70, and 72 are about writing data block to disk if the data block has the lowest cost function, overwriting cached read data with new data block if the read command type has the lowest cost function and writing cached write data to disk and overwriting cached write data block with new data block if the write command type has the lowest cost function. The cited FIG. 4, references 96, 100, 102, and 104 are about not storing the data block in cache if the data block has the lowest cost function and overwriting cached read data with new data block if the read command type has the lowest cost function, writing cached write data to disk and overwriting cached write data with new data block if the write command type has the lowest cost function.

The cited col. 4 lines 29-55 disclose managing a cache based on the access time of the command under consideration wherein if a data block has a higher access time, it is preferably kept or added into cache while data with a lower access time is preferably not stored in cache.

As can be seen, these cited references do not disclose determining an access time to acquire the piece of data in the memory system. These cited references do not disclose a threshold, wherein a value of the threshold is selected based on whether the value is a realistic time for a memory access. As a result, these cited paragraphs cannot logically disclose comparing the determined access time to the threshold.

Further, neither does Lamberts disclose the following limitations:

"a memory table includes entries pointing to data blocks storing data for at least one subsystem;

the entries are used to locate the data stored in the data blocks; and

while the first process is being executed, the memory table working with a memory manager manages the data blocks independent of an operating system working with the memory system and independent of a processor working with the memory system"

Regarding claims 2 and 24, the Office Action cited FIG. 5 and column 9, line 24 through column 10, line 28. FIG. 5 shows the locations of data corresponding to commands in the command queue (col. 9, lines 25, 26), but does not disclose the claimed limitation that "the data block containing the piece of data is placed in the memory system based on information selected in one or a combination of a movement pattern of data in the data block, a structure of the memory system, and a cache level architecture in the memory system." The cited paragraph of col. 9, line 24 through col. 10, line 28, even though mentions "data blocks," but discusses "the probability that a future read command references the data block . . . is proportional to the

instantaneous cache hit ration, either an average value or the value for the particular data block" (col. 10, lines 12-15), which has no bearing on the claimed limitation as recited.

Regarding claims 13-14, the Office Action asserted that "Lamberts teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103 – Hughes and Frank

In paragraphs 9 and 10, claims 3-5, 15-17 and 25-27 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hughes and U.S. patent number 5,297,265 to Frank ("Frank"). The alleged motivation for combination is improper and Frank does not provide the claimed limitations missing in Hughes. Therefore, showing a prima facie case of obviousness failed, and the claimed invention is patentably distinguished from Hughes and Frank, either alone or in combination.

Regarding claims 3-5 and 25-27, the assertion that "it would have been obvious . . . implement the system and method for managing a memory system as taught by Hughes to utilize a memory table as taught by Frank to improve data coherency, which requires little or no software overhead, as well as reducing memory access latency and bus contention providing a multiprocessing system with unlimited scalability as pointed out by Frank on column 2, line 27 through line 37" is improper because it is merely a broad conclusory statement of Frank, and no evidence that suggests the combination was provided. Therefore, the alleged motivation is insufficient to support a prima facie case of obviousness.

The limitations of canceled claims 3 and 4 are now in claim 1. However, Frank does not disclose such limitations as asserted in the Office Action. For example, Frank does not disclose a "memory manager." Frank does not disclose "the memory table working with the memory manager manages the data blocks." Frank does not disclose such management of the data blocks is "independent of an operating system working with the memory system and independent of a processor working with the memory system" while the first process is being executed. Frank does not disclose the limitation in claim 5, either.

Regarding claims 15-17, the Office Action asserted that "Hughes teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103 – Lamberts and Eickemeyer

In paragraph 11, claims 6-8, 11, 18-19, 21, 28-29, and 31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lamberts and U.S. patent number 6,049,867) to Eickemeyer ("Eickemeyer"). The rejection is traversed because the alleged motivation for combination is improper, Eickemeyer does not provide the claimed limitations missing in Lamberts, and therefore showing a prima facie case of obviousness failed.

Regarding claims 6-8, 11, 28-29, and 31 the Office Action cited Lamberts' Figure 3 and Figure 4. The Office Action admitted that "Lamberts does not specifically teach the method of accessing the memory system for a piece of data used by the first process, a processor working with the memory system continuing its

function until it is stalled." The Office Action then asserted "Eickemeyer teaches a system and method for memory management to reducing memory access latency utilizing a process or thread to allow the switching between multiple threads in response to the occurrence of an event such as a cache miss or stall that indicates long memory latency may occur. In an event of a cache miss, a first thread is suspended allowing a second thread to access the cache memory."

Regarding claim 6, 18, and 28, the Office Action admitted that Lamberts does not teach "[upon accessing the memory system for a piece of data used by a first process,] a processor working with the memory system continuing its functions until it is stalled." However, no evidence was provided to show that Eickemeyer provides this limitation missing in Lamberts. Therefore, a prima facie case of obviousness by combining Lamberts and Eickemeyer failed.

The amended claimed invention also includes the limitation "comparing a time taken to complete the memory access to a threshold . . .; a value of the threshold is selected based on whether the value is a realistic time for a memory access," which is not provided in Lamberts, nor cured by Eickemeyer. Therefore, the claimed invention is patentably distinguished from Lamberts or Eickemeyer, alone or in combination.

Even though the limitation "if the time taken to complete the memory access is close to, equal to, or greater than the threshold" is being canceled, it is for the record that neither Lamberts nor Eickemeyer discloses this limitation. The invention is amended to claim in alternative languages, not because the prior taught the claimed limitation.

The alleged motivation for combining lamberts and Eickemeyer is improper because the assertion that "the utilization of a process switch provides further memory access latency reduction and eliminates the need for complex, replication of pipeline latches and pipeline states rendering a cost effective system" is conclusory without

specificity related to Lamberts. This assertion, if any, is utilized by Eickemeyer, but does not suggest the motivation for combining the two teachings of Lamberts and Eickemeyer. Therefore, a prima facie case of obviousness for combining the two teachings failed.

Regarding claim 7, even though Eickemeyer discusses switching between multiple threads, as discussed, the alleged motivation for combination failed. Further, Eickemeyer does not teach switching the processes in the context of other limitations in claim 6. Both Lamberts and Eickemeyer do not disclose causing a performance monitor on the memory system or on a system using the memory subsystem.

Regarding claims 8, 19, and 20 Eickemeyer does not disclose a latency manager being part of managing the memory system. Eickemeyer does not disclose polling the latency manager for the time taken to complete the memory access.

Regarding claims 11, 21 and 31, both Lamberts and Eickemeyer do not disclose the additional limitation "counting a time elapsed from the time the data access starts; the counted time being increased as the data is being accessed." Other limitations in these claims are not disclosed in Lamberts as discussed above. They are not disclosed in Eickemeyer, either. Even though the limitation "if the counted time is close to, equal to, or greater than the threshold" is being canceled, it is for the record that this limitation is not disclose in Lamberts nor Eickemeyer. The claim is amended to claim in alternative language, not because the prior art disclosed the limitation.

Regarding claims 18-19 and 21, the Office Action asserted that "Lamberts teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103 – Lamberts, Eickemeyer and Frank

In paragraph 12, claims 9-10, 12, 20, 22, 30, and 32 were rejected under 35 U.S.C 103(a) as being unpatentable over Lamberts and Eickemeyer as applied to claim 6, 11, 18, 21, 28 and 31, and further in view of Frank. The alleged motivation for combination is improper. Further, Lamberts, Eickemeyer, and Frankd do not provide the claimed limitations either alone or in combination, and therefore showing a prima facie case of obviousness failed. As discussed above, the alleged motivation for combining the teaching of Lamberts and Eickemeyer was improper. The alleged motivation for combining Frank was also improper, and therefore showing of a prima facie case of obviousness failed.

Regarding claims 20 and 22, the Office Action asserted that "Lamberts teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

ADDED CLAIMS

Claims 33-35 are being added, which depend from claims 5, 17, and 27, respectively, and are therefore patentable for at least the same reasons as claims 5, 17, and 27, respectively. Claims 5, 17, and 27 are also patentable for their limitations not taught in the prior art of record, including "wherein the physical address of the memory page is converted from a virtual address of the piece of data." Applicants respectfully submit that limitations in claims 33-35 are supported in the Specification, and therefore no new matter is added.

SUMMARY

In conclusion, pending and added claims clearly present subject matter that is patentable over the prior art of record, and therefore withdrawal of the rejections and consideration of the added claims are respectfully requested.

Respectfully submitted,

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